WHAT IS CLAIMED IS:

1. A logic circuit diagram input device for estimating a layout area based on a logic circuit diagram constituted by a transistor as a minimum unit, comprising:

hierarchy developing means for developing logic circuit diagram information having a hierarchical structure to information at a transistor level;

configuration parameter information extracting means for extracting configuration parameter information such as a gate length, a gate width, a drain region area and a source region area which are added to each transistor as a property;

area calculating means for calculating each transistor area using a transistor area calculation formula for calculating a transistor area from the said configuration parameter information; and

layout area estimating means for estimating a layout area by adding all areas of the transistors together.

2. A logic circuit diagram input device according to claim 1, wherein said each transistor area is corrected using an area possession ratio per predefined transistor.

3. A logic circuit diagram input device for estimating a layout area based on a logic circuit diagram constituted by a standard cell, comprising:

hierarchy developing means for developing logic circuit diagram information having a hierarchical structure to information at a standard cell level;

an each standard cell area holding part for holding each standard cell

area according to an instance;

area deriving means for deriving said developed each standard cell area according to the instance of the cell based on data of said each standard cell area holding part; and

layout area estimating means for estimating the layout area by adding all of the areas of the standard cells.

4. A logic circuit diagram input device according to claim 3, wherein said each standard cell area is corrected using an area possession ratio defined for each kind of the standard cell.

5. A logic circuit diagram input device according to claim 3, comprising:

wiring information extracting means for extracting wiring information from said logic circuit diagram information having the hierarchical structure; and

probable wiring possession area value holding means for holding a probable value of a wiring possession area, which is defined according to a layout area and the number of cells, wherein the sum of the probable values of the wiring possession areas which were extracted from the probable wiring possession area value holding means per wiring is added to said layout area.

6. A logic circuit diagram input device according to claim 5, comprising:

each block area wiring capacity of holding part for holding a probable wiring capacity value defined according to a layout area and the number of cells; and

probable wiring capacity value extracting means for extracting probable wiring capacity value from said each block area wiring capacity holding part per wiring.

7. A logic circuit diagram input device according to claim 6, wherein information of said probable wiring capacity value is added to wiring data on the logic circuit diagram constituted by a standard cell as a property or an element.

8. A logic circuit diagram input device according to claim 1, wherein further detailed physical information such as a maximum gate width, a unit resistance value, a unit capacity value or the like is added other than configuration parameter such as a gate length, a gate width, a drain region area and source region area which were added to a transistor element as a property.

9. A logic circuit diagram input device according to claim 2, wherein an area possession ratio is set on higher level of block in stead of an area possession ratio set per transistor.

10. A logic circuit diagram input device according to claim 1, wherein each cell, a block area and the number of basic cells (BC) which were estimated by the device are provided to a layout designing apparatus as an input file.

11. A logic circuit diagram input device according to claim 1, wherein each cell, a block area and the number of basic cells (BC) which were estimated by the device are stored in each instance element on a logic circuit diagram as a property.